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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/879,208 | 06/13/2001 | Yukihito Oowaki | 02887.0141-01000 | 4453 |

22852 7590 06/20/2003

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| EXAMINER | |
|---|---|
| RAO, SHRINIVAS H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 06/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/879,208 | OOWAKI ET AL. | |
| | Examiner | Art Unit | |
| | Steven H. Rao | 2814 | |

*-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *25 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *14-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *14-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Respons to Am ndment***

Applicants' amendment filed on April 23, 2003 has been entered on April 25, 2003.

Therefore claims 14,18, 22 and 27 as amended by the amendment and claims 15-17, 19-21, 23-26,28-33 as previously recited are currently pending in the Application.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 14 –33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants' have amended independent claims 14,18,22 and 27 and therefore claims 14-31 to recite , " removing said second film to form a second groove in the semiconductor substrate " ( underlined portion added by the present amendment) .

The application as originally filed does not describe and the drawings do not show the second groove to be in the semiconductor substrate , but rather describe(

Specification pages 13-14, etc.) and show ( as best seen in figures 4 D and E , and 13 that the second groove formed by removing the second film (3) is formed on top of the substrate(1) above the channel region and near the top of the first film (12) which is over semiconductor substrate (1) and not in the semiconductor substrate (1) .

Therefore the formation of the second groove in the semiconductor substrate is not described/shown in the specification/drawings as originally filed.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

Claims 14-31 re rejected under 35 U.S.C. 103(a) as being unpatentable over Shin ( U.S. Patent No. 5,270,257 herein after Shin) and Kirvokapic ( U. S. Patent No. 6,025,635, herein after Kirvokapic) all previously applied.

With respect to claims 14, (assuming arguendo applicants' over come the new matter rejection) Shin and Krivokapic teach a method of forming a MIS transistor including a semiconductor substrate ( Shin fig. 3a #21, col. 4 line 19), source/drain regions ( Shin fig.3c # 26b and 26a, col.4 lines 46-47) formed on the substrate and a gate electrode provided above a channel region between the source/drain regions (Shin fig. 3b #24, col. 4 line 41and region below gate 24 and oxide 23) the method comprising : selectively forming a first film on the semiconductor substrate ( Shin Fig. 3 c-e # 22- nitride) , etching the semiconductor substrate to form the first groove by using the first film as a mask ( Shin Fig. 3A), forming a second film in the first groove (Shin fig. 3b # 23/25) and thereafter removing the first film (Shin Fig. 3 C), diffusing an

impurity on a surface of the semiconductor substrate to form a grooved impurity diffusion region including a part thereof extending below the first groove by using the second film as a mask.

Shin does not specifically disclose the steps of forming an impurity diffusion region including a part of a bottom of the first groove ( i.e. an impurity diffusion region including a part thereof extending below the first groove ) and an insulator film on the grooved impurity diffusion region and thereafter removing the second film to from a second groove in the semiconductor substrate.

However, Krivokapic, a patent from the same filed of endeavor, describes in figs. 13 col. 7 lines 6 to 20 forming an impurity diffusion region including a part of a bottom of the first groove to form self-aligned source/drain regions in small channel length devices and in figures 8, 9 and 15 and col.6 lines 15-27 and col. 7 lines 26-49 the forming an insulator film on the grooved impurity diffusion region and thereafter removing the second film to from a second groove to form an extremely small channel length transistor.

Therefore it would have been obvious for one of ordinary skill in the art at the time of the invention to Include Kirvokapic's step of forming an impurity diffusion region including a part of a bottom of the first groove to form self-aligned source/drain regions in small channel length devices and forming an insulator film on the grooved impurity diffusion region and thereafter removing the second film to from a second groove to from a second groove to form an extremely small channel length transistor. ( Krivokapic col. 3 lines 64-67).

Forming a gate insulator film in the second groove so that the top surface of the gate insulator film is higher than a top surface of said impurity diffusion region ( Kirvokapic fig.12 # 205, col. 7 lines 4-5) and forming a gate electrode on top of the gate insulator film ( Krivokapic fig. 14 # 242).

With respect to claim 15, wherein the second film is semiconductor film ( Shin film 24 is poly silicon , Shin col. 4 line 41) and forming a sacrificial film in the first groove before forming the second film in the first groove ( Krivokapic figs. 8 and 9 # 200).removing the sacrificial film after removing the second film to form the second groove. ( Krivokapic fig. 9 and 10).

With respect to claim16, wherein a step of polishing a surface of the second film by using the first film as a stopper ( Shin fig. 11, col. 6 lines 66-67).

With respect to claim 17, forming a protective film in the second groove before forming the gate insulator film in the second groove ( Shin fig. 14 # 285).

With respect to claim 18, it repeats all the steps of claim 14 ( see above) and further includes the step of : polishing the gate insulator film by using the insulator film as a stopper (Shin fig. 11, col. 6 lines 66-67).

Claims 19-21 repeat the steps of claims 15-17 and are rejected for reasons set forth above.

Claim 22 repeats the steps of claim 18 except for the absence of the second film-forming step and is rejected for reasons stated under claim 18 above.

Claims 23 wherein the source/ drain regions are elevated by an epitaxial growth technique before the diffusion step. ( fig. 3 e # 28a and b, col. 4 lines 65-68).

With respect to claim 24, wherein the a diffusing step is carried out before elevating the source/drain region by epitaxial growth. ( See above claim 23 and further it is well settled that changing the order of performing the methods steps is prima facie obvious unless the change in the sequence of steps can be shown to produce unexpected results or is critical to the method).

It is also noted that the specification contains no disclosure of either the critical nature of the claim sequence of steps or any unexpected results arising there form. Where patenability is said to be based upon particular chosen dimensions or upon variable recited in a claim, the Applicant must show the chosen sequence are critical. In re Woodruff, 919 F.2D. 1575, 1578, 16 USPQ 2d 1934, 1936 ( Fed. Cir. 1990).

Claims 25-26 repeat the steps of claims 19 and 21 above and are rejected for reasons stated above.

With respect to claim 27, repeats the steps of claims 18 and 22 and is rejected for reasons set out above.

Claims 28-31 repeat the steps of claims 23, 24, 25 and 26 and are rejected for reasons set out above.

With respect to claim 32 , in addition to the steps of claims 18 and 22, claim 32 further recites the source/drain regions forming an inclined surface between the top surface of the semiconductor layers and the channel region ( Shin fig. 3e # 26a and b) , forming a dummy film on the channel region that borders the semiconductor layers ( part of 24 etched away).

Depositing a gate electrode on a top side of the gate insulator film to form a gate electrode having a cross section of a T shape.

Krivokapic describes the forming of a gate electrode on a top side of the gate insulator film to form a gate electrode . ( Krivokapic fig. 14 # 242).

Krivokapic does not specifically describe the gate having a cross section of a T-shape .

However, Lee, a patent from the same filed of endeavor, describes in fig. 3 B-D and col. 5 lines 7-8 describes a metal layer and a damascene structure that has a T-shaped cross-section to form a circuit/device with improved speed and avoiding logical cross-talk errors.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lee's interconnect having a T-shaped cross section in Krivokapic method to form a circuit/device with improved speed and avoiding logical cross-talk errors. ( Lee col. 1 lines 41-44).

Claims 33 repeat the steps of claims 14 and 22,23, 28 and are rejected for the reasons set out above.

**Response to Arguments**

Applicant's arguments filed 9/13/02 have been fully considered but they are not persuasive for the following reasons :

Applicants' contend that Shin does not teach/suggest at least forming an insulator film on an impurity diffusion region ( as stated in the O/A page 4 , 1st. full paragraph) and further Krivokapic does not cure the deficiencies of Shin because Kirvokapic does not describe/suggest " forming an insulator film on an impurity diffusion region and therafter removing a second film to form a second groove is not persuasive because Krivokapic figure 9 reproduced below shows formation of an insulator film ( 215) on an impurity diffusion region ( fig. 9 ) and thereafter removing a second film ( 205) to form a second groove ( fig. 9 , 200a ) in the semiconductor substrate ( it is noted that the phrase " in the semiconductor substrate is new matter) and etching step ( removal) can be done either before implantat1on ( first embodiment) or after implantation ( i.e. after forming an impurity region and on it in a second embodiment , also reproduced below) which is similar to Applicants' description/drawings in figs. 4, 13 and specification pages 13-14.

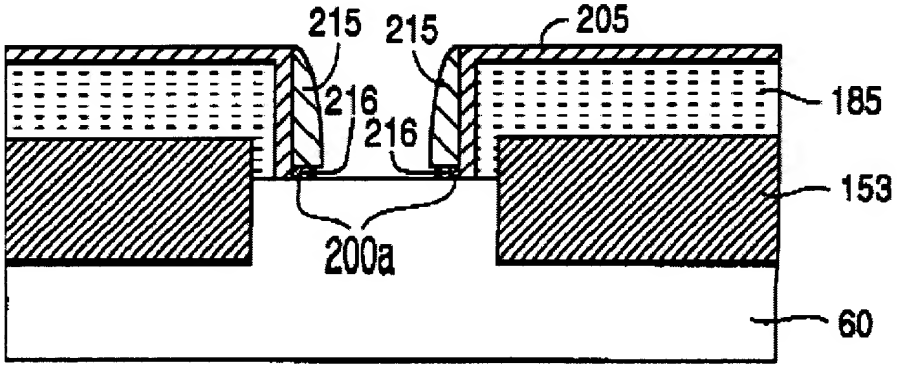



FIG. 9

and in col. 6 line 36 to 39 states :

tional techniques. (It should be recognized that in an alternative embodiment, the step of etching oxide 200 may occur subsequent to the following implants). A first implant is used [illegible] ( removal) is carried out after the implantation ( see above) the oxide layer 200 will be formed on an impurity region ( i.e. implanted region) .

Further Kirvokapic's above embodiment describes thereafter ( i.e. after implantation and forming an insulator film on an impurity diffusion region) removing a second film ( part of film 200 etched to leave 200a in figure 9) to form a second groove ( 200a) .

Applicants' arguments that Kirvokapic's grooves are formed on the surface of the substrate and not in the substrate is not persuasive because as stated above Applicants' disclosure also only supports forming the second groove on the surface of the substrate ( see e.g. Applicants' figures 4D,E and 13 and specification pages 13-14).

Further, Shin in figure 3 c describes forming grooves in the substrate.

Applicants' allegation that it would be inconsistent to include the teachings of Kirvokapic in Shin's method steps because it would yield an un desirable instance of having an exposed region of the semiconductor substrate before the step of ion – injection to make the source and drain regions is not persuasive because Kirvokapic itself describes in its first embodiment channel implants after removal of layer 200 to expose a region of the semiconductor through which the ions are implanted. ( Kirvokapic col. 6 lines 29-40 and figure 10).

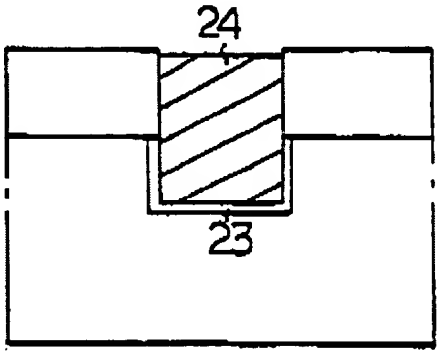
Applicants' contention that Shin and Kivokapic were combined without particularized motivation is not persuasive because the particular motivation was previously and is currently set out several times to be :

form self-aligned source/drain regions in small channel length devices and forming an insulator film on the grooved impurity diffusion region and thereafter removing the second film to from a second groove to from a second groove to form an extremely small channel length transistor. ( Krivokapic col. 3 lines 64-67).

Therefore Applicants' arguments with regard to claims 15-17 and 19 –21 are not persuasive.

Applicants' contention that Kirvokapic does not teach/ suggest , " forming a gate insulator in the groove in the semiconductor substrate so that a top surface of said gate insulator is higher than a top surface of an impurity diffusion region" is not persuasive because the rejection is based upon the combined teachings of Shin and Kirvokapic and shin in figures 3 b to 3e shows layer ( 23/25/27) all within the substrate . ( Shin figure 3b reproduced below).

F I G. 3b



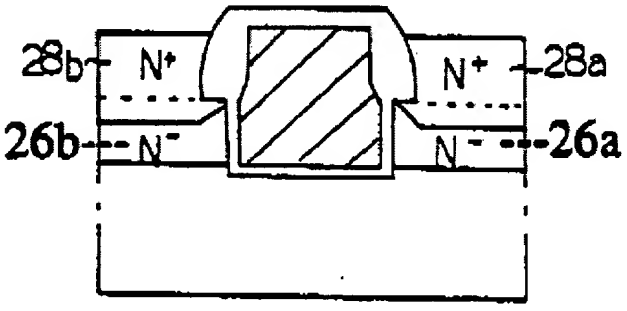
Therefore Applicants' arguments with respect to claim 22 are not persuasive.

Applicants' repeat the argument Shin and Kirvokapic do not teach" forming an insulator film on said impurity diffusion region; removing a first film so as to form a groove in the semiconductor substrate and forming a gate insulator in said groove in the semiconductor substrate and on said insulator film " is not persuasive for reasons stated above and incorporated here by reference for the sake of brevity.

Therefore Applicants' arguments with reference to claims 22-26 and 27-31 are not persuasive.

Applicants' contention that Kirokapic does not show an inclined surface between the top surface of the semiconductor substrate and a channel region is not persuasive because the previous rejection was based on Shin fig. 3e # 26 a and b ( see previous O/A/ mailed 01/23/2003 page 6 lines last seven lines ( from bottom) and Shin figure 3 e reproduced below.

F I G. 3e




Therefore Applicants' contention with regards to claims 32-33 are not persuasive

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7463926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner.

June 16, 2003.

SUPERVISORY PATENT EXAMINER
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